

$$\begin{array}{ccccccc} \mathbf{31A} & & \mathbf{32A} & & \mathbf{33A} & & \mathbf{34A} \\ | & & | & & | & & | \\ \text{CHA\_OUT} = \text{CHA\_SOURCE} & + & [\text{K}_1 * (\text{CHB\_SOURCE\_delayed\_by\_D1})] & - & [\text{K}_2 * (\text{CHA\_SOURCE\_delayed\_by\_D2})] \\ & & & & & & \\ & & \mathbf{35A} & & \mathbf{36A} & & \mathbf{37A} \\ & & | & & | & & | \\ & & - [\text{K}_3 * (\text{CHB\_SOURCE\_delayed\_by\_D3})] & + & [\text{K}_4 * (\text{CHA\_SOURCE\_delayed\_by\_D4})] & + & \dots \end{array}$$

**Fig. 1 A**

$$\begin{array}{ccccccc} \mathbf{31B} & & \mathbf{32B} & & \mathbf{33B} & & \mathbf{34B} \\ | & & | & & | & & | \\ \text{CHB\_OUT} = \text{CHB\_SOURCE} & - & [\text{K}_5 * (\text{CHA\_SOURCE\_delayed\_by\_D5})] & - & [\text{K}_6 * (\text{CHB\_SOURCE\_delayed\_by\_D6})] \\ & & \mathbf{35B} & & \mathbf{36B} & & \mathbf{37B} \\ & & | & & | & & | \\ & & + [\text{K}_7 * (\text{CHA\_SOURCE\_delayed\_by\_D7})] & + & [\text{K}_8 * (\text{CHB\_SOURCE\_delayed\_by\_D8})] & - & \dots \end{array}$$

**Fig. 1B**

$$\text{SURROUND\_A\_OUT} = - [\text{K}_9 * (\text{CHB\_SOURCE\_delayed\_by\_D9})] + [\text{K}_{10} * (\text{CHA\_SOURCE\_delayed\_by\_D10})] \\ + [\text{K}_{11} * (\text{CHB\_SOURCE\_delayed\_by\_D11})] - \dots$$

**FIG. 1C**

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$$\begin{aligned} \text{SURROUND\_B\_OUT} = & [K_{12} * (\text{CHA\_SOURCE\_delayed\_by\_D12})] + [K_{13} * (\text{CHB\_SOURCE\_delayed\_by\_D13})] \\ & - [K_{14} * (\text{CHA\_SOURCE\_delayed\_by\_D14})] - \dots \end{aligned}$$

Fig. 1 D

$$\begin{aligned} \text{SURROUND\_A\_OUT} = & - [K_9 * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D9}})] \\ & + [K_{10} * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D10}})] \\ & + [K_{11} * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D11}})] - \dots \end{aligned}$$

Fig. 1 E

$$\begin{aligned} \text{SURROUND\_B\_OUT} = & + [K_{12} * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D12}})] \\ & + [K_{13} * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D13}})] \\ & - [K_{14} * ((\text{CHA\_SOURCE-CHB\_SOURCE})_{\text{delayed\_by\_D14}})] - \dots \end{aligned}$$

Fig. 1 F

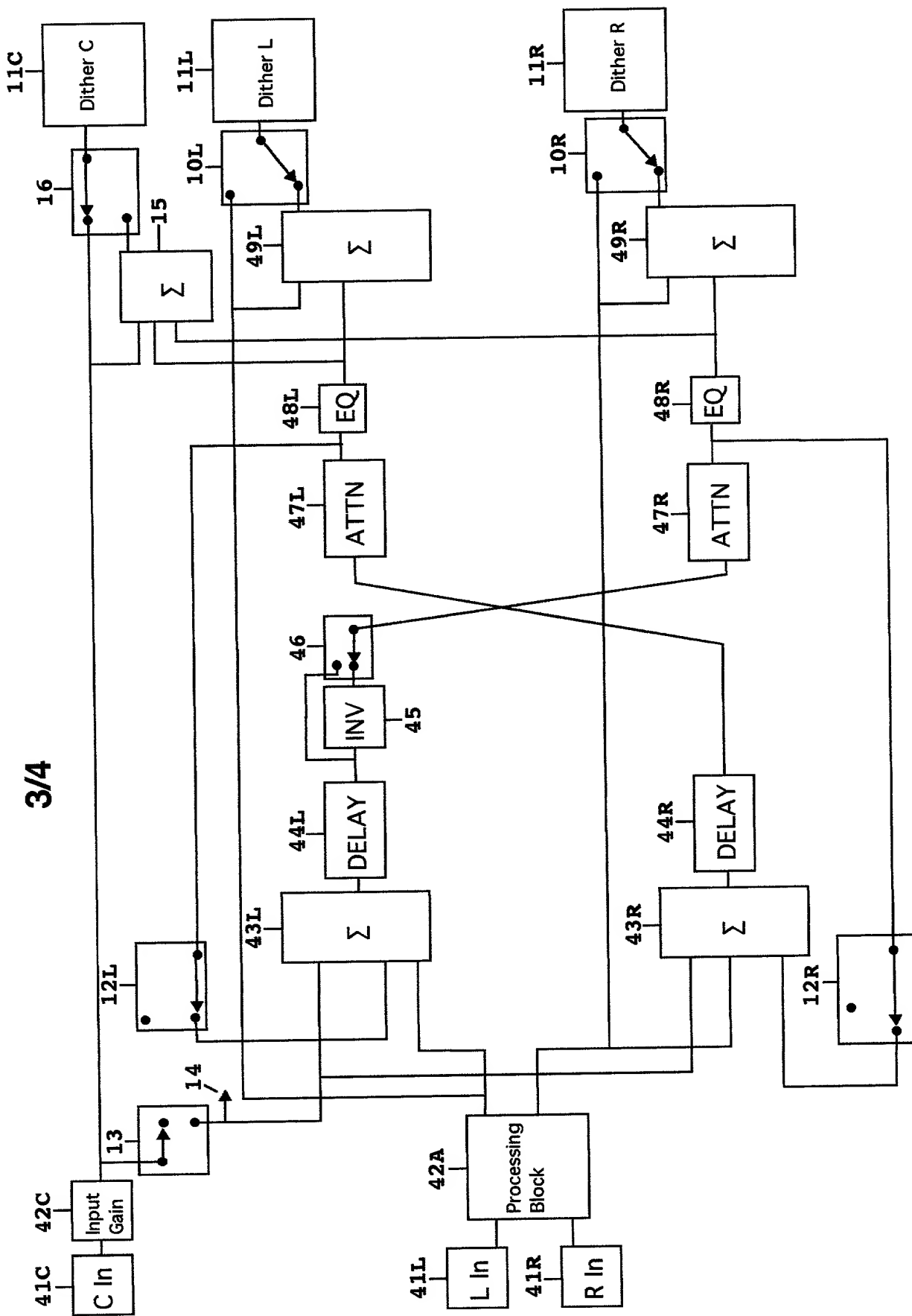


Fig. 2

FIG. 3 is a block diagram of a 4/4 channel audio processor. The diagram shows the signal flow from inputs (41LS, 41RS, 41LFE) through various processing blocks (42LS, 42RS, 42LFE, 17, 18A, 18B, 19A, 19B, 20, 21A, 21B, 22A, 22B, 23A, 23B, 24A, 24B) to outputs (11LS, 11RS, 11LFE). The central processing section includes a Surround Feed Switch (17) and two summing junctions (18A, 18B). The output section includes two summing junctions (23A, 23B) and two delay blocks (19A, 19B). The diagram is labeled 4/4 in the center.

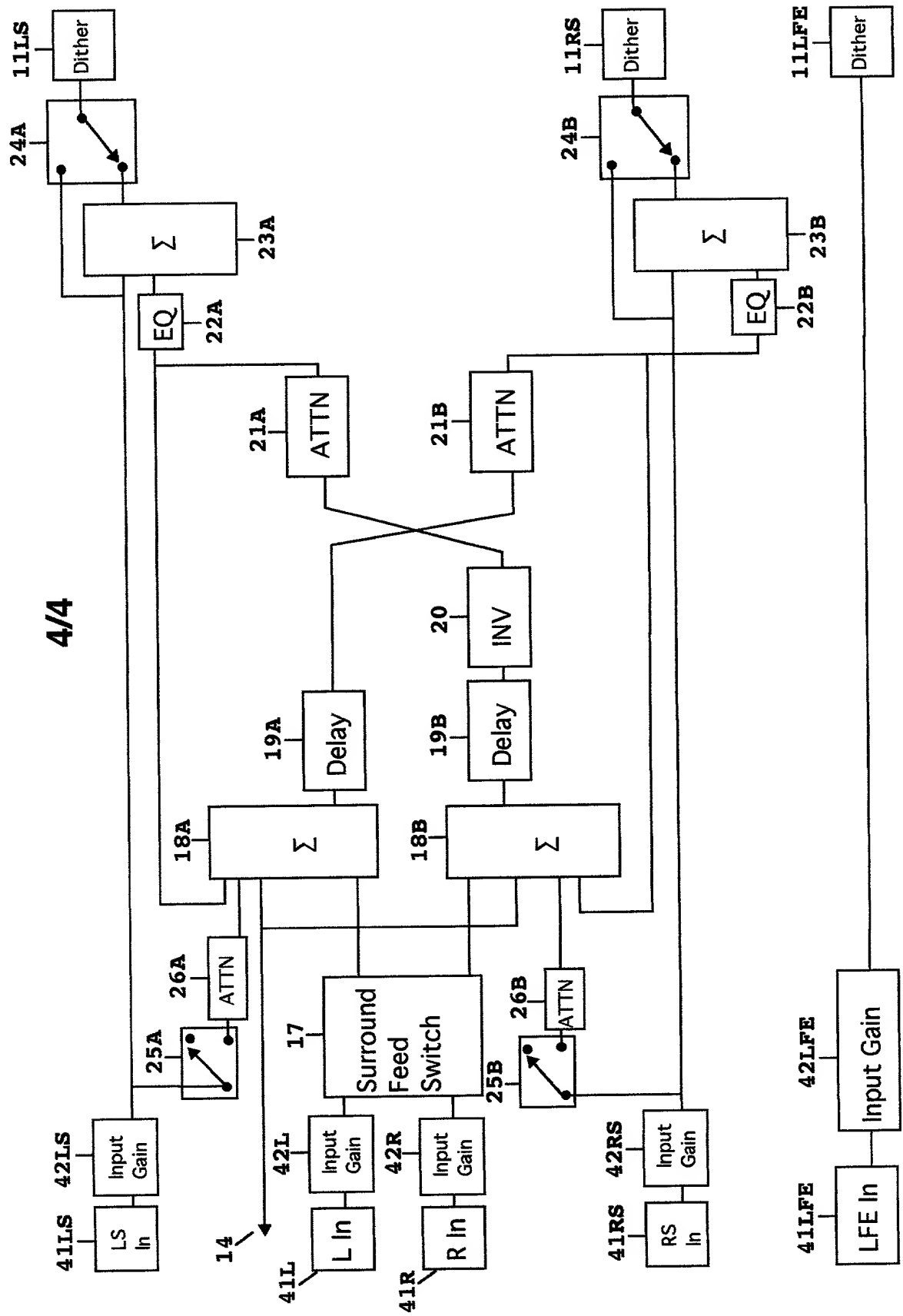


Fig. 3